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| 10/566,955 | 08/21/2006 | Volker Harle | 5367-220PUS | 9357 |
| 27799 7590 04/14/2008 COHEN, PONTANI, LIEBERMAN & PAVANE 551 FIFTH AVENUE SUITE 1210 NEW YORK, NY 10176 | | | | |
| EXAMINER HUNG, MING HUNG | | | | |
| ART UNIT 2829 | | PAPER NUMBER | | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/566,955

Applicant(s)

HARLE, VOLKER

Examiner

MING HUNG HUNG

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/ICE)
- Paper No(s)/Mail Date 01/30/06
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. Preliminary amendment received on 01/30/06 has been entered into record.

Priority

2. Examiner acknowledged that this application 10/566,955 filed on 08/21/06 claims the benefit of the foreign application DE 103 35 080.2 filed on 07/31/03. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed 01/30/06 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the English abstract for DE 102 06 751 A1 published on 07/03/02 was not provided. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Objections

4. Claims 6, 11 and 12 are objected to because of the following informalities:
- a. As to claim 6, line 3, "the active zone" lacks antecedent basis. "the active zone" should read "an active zone".
 - b. As to claim 11, it fails to further limit the preceding claim because any material has dielectric properties.
 - c. As to claim 12, lines 3-4, the addition of "like" renders the claim indefinite. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-8, 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haerle (US Patent No. 6,100,104) in view of Shi et al. (US Patent No. 5,693,962 and Shi hereinafter).
7. As to claim 1, Haerle discloses:
- a method for the production of a plurality of optoelectronic semiconductor chips** (a plurality light emitting diode chips 100 as shown in Figs. 5-6) **each having a**

plurality of structural elements with respectively at least one semiconductor layer (21, 23, and 22 as shown in Fig. 5; col. 7, lines 1-5), **comprising the steps of:**
providing a chip composite base (substrate wafer 19, Figs. 1-3) **having a substrate** (growth substrate wafer 3, Figs. 1-5) **and a growth surface** (the main surface 9, Fig. 1);
forming a mask material layer on the growth surface (mask layer 4, Fig. 1), **with a multiplicity of windows** (mask openings 10, Fig. 3), **where a mask material being is chosen in such a way that a semiconductor material of the semiconductor layer that is to be grown in a later method step essentially cannot grow on said mask material or can grow in a substantially worse manner in comparison with the growth surface** (col. 6, lines 55-67); **essentially simultaneously growing semiconductor layers on regions of the growth surface that lie within the windows** (Fig. 4); **and singulating the chip composite base with applied material to form semiconductor chips** (col. 7, lines 33-36; Figs. 5-6).

However, Haerle fails to disclose:

most of windows have an average extent less than or equal to 1 μm .

Nonetheless, this feature is well known the art and would have been an obvious modification of the method disclosed by Haerle, as evidenced by Shi.

Shi discloses a full color organic light emitting diode array comprising:

most of windows have an average extent less than or equal to 1 μm (col. 4, lines 15-27; col. 5, line 66-col. 6, line 8; Examiner interprets the average extent being the depth of the windows).

Given the teaching of Shi, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Haerle by employing the well known or conventional feature of windows with an average extent less than or equal to 1 μm , such as disclosed by Shi, in order to produce a display with the desired size and resolution easily.

8. As to claims 2-8, 12-14, Haerle also discloses:

the chip composite base (substrate wafer 19, Figs. 1-3) has at least one semiconductor layer grown epitaxially onto the substrate (col. 6, line 55-col. 7, line 5) and the growth surface is a surface on that side of the epitaxially grown semiconductor layer (the bottom side of 21 is in contact with the main surface 9 as shown in Fig. 4) which is remote from the substrate (col. 6, lines 52-53) [claim 2];

the chip composite base (substrate wafer 19, Figs. 1-3) has a semiconductor layer sequence grown epitaxially onto the substrate (col. 6, line 55-col. 7, line 5) with an active zone that emits electromagnetic radiation (light-emitting active layer 23, Fig. 4), and the growth surface is a surface on that side of the semiconductor layer sequence (the bottom side of 21 is in contact with the main surface 9 as shown in Fig. 4) which is remote from the substrate (co. 6, lines 52-53) [claim 3];

the structural elements respectively have an epitaxially grown semiconductor layer sequence (col. 6, line 55-col. 7, line 5) with an active zone that emits electromagnetic radiation (light emitting active layer 23, Fig. 4) [claim 4];

the mask material has SiO_2 , Si_xN_y or Al_2O_3 (col. 6, lines 38-39) [claim 5];

after the growth of the semiconductor layers (Fig. 5 is performed after Fig. 4), **a layer made of electrically conductive contact material that is transmissive** (front-side contact metallization layer 15, Fig. 5; it is transmissive because it would either bounce the radiation when a non-transparent material is used or pass the radiation through when a transparent material is used) **to an electromagnetic radiation emitted by the active zone** (light-emitting active layer 23, Fig. 4) **is applied to the semiconductor layers, so that semiconductor layers of a plurality of structural elements are electrically conductively connected to one another by the contact material** (they are electrically conductively connected because the front-side contact metallization layer 15 is a conductor) **[claim 6];**

the average thickness of the mask material layer (mask layer 4, Fig. 9) **is less than the cumulated thickness of the semiconductor layers of a structural element** (semiconductor layer sequence 18, Fig. 9) **[claim 7];**

the mask material layer is at least partly removed after the growth of the semiconductor layers (col. 7, lines 13-20) **[claim 8];**

the growth conditions for the growth of the semiconductor layers are set and/or varied during growth in such a way that semiconductor layers of the structural elements form a lenslike, a truncated-conelike or a polyhedral form (col. 7, lines 66-67) **[claim 12];**

the semiconductor layers are grown by means of metal organic vapor phase epitaxy (col. 6, lines 55-67) **[claim 13];**

an optoelectronic semiconductor chip, characterized in that it is produced according to a method as claimed in claim 1 (col. 7, lines 33-36) [claim 14].

9. Claim 9-11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haerle in view of Shi as applied to claim 1, and further in view of Braun (US Patent No. 6,110,277, Applicant's admitted prior art).

Although Haerle in view of Shi discloses substantial features of the claimed invention, it fails to disclose:

after the growth of the semiconductor layer sequences, a planarization layer is applied over the growth surface [claim 9];

a material whose refractive index is lower than that of the semiconductor layers is chosen for the planarization layer [claim 10];

a material which has dielectric properties is chosen for the planarization layer [claim 11].

Nonetheless, these features are well know in the art and would have been an obvious modification of the method disclosed by Haerle in view of Shi, as evidenced by Braun.

Braun discloses a process for the fabrication of epitaxial layers of a compound semiconductor on monocrystal silicon and light-emitting diode fabricated therefrom comprising:

after the growth of the semiconductor layer sequences, a planarization layer is applied over the growth surface (passivation layer 60, Fig. 5) **[claim 9]** to protect the light-emitting diode;

a material whose refractive index is lower than that of the semiconductor layers is chosen for the planarization layer (the passivation layer 60 in Fig. 5 must have a refractive index that is lower than the semiconductor layers to allow the radiation to pass through, otherwise the radiation is blocked and the light-emitting-diode could not shine) **[claim 10];**

a material which has dielectric properties is chosen for the planarization layer (any material has dielectric properties, including the passivation layer 60 in Fig. 5) **[claim 11].**

Given the teaching of Braun, person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Haerle in view of Shi by employing the well known or conventional features of a lower refractive index planarization layer, such as disclosed by Braun, in order to make a light-emitting diode with extraordinary efficiency and optimized green, blue, and violet spectral region.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ming Hung Hung whose telephone number is (571) 270-3832. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ming Hung Hung/
Examiner, Art Unit 2829
04/09/08

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829